

Automatic Balancing of Flying Capacitor Voltages through Deterministic Switching States

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Abstract—This work investigates the inherent deterministic behavior exhibited by certain switched-capacitor networks and explores how it can be leveraged within hybrid switched-capacitor (HSC) power converter topologies. These networks are able to impose deterministic flying capacitor voltage biases *without* interacting with the under-damped inductor(s) required for soft-charging and subsequent high conversion efficiency. This enables flying capacitor voltages to rapidly and appropriately rebias with changes in line voltage, ensuring correct distribution of voltage stress among all components within the converter. Importantly, we demonstrate that this intrinsic self-biasing mechanism can be lossless in periodic steady-state, under both loaded and unloaded conditions. As a case study, we demonstrate a *deterministic interleaved* flying capacitor multilevel (DI-FCML) converter in hardware—a structure in which the switched-capacitor networks of two conventional FCML converters share a single output LC filter. We present one appropriate clocking scheme for fixed-ratio conversion that employs split-phase switching and imposes deterministic voltage biases by design, without increasing switching activity. Hardware results confirm that soft-charging is preserved in steady-state and illustrate automatic flying capacitor voltage rebiasing within four switching periods when subject to a rapid 100% line voltage increase.

Index Terms—switched-capacitor converter, flying-capacitor multi-level (FCML), voltage balancing, split-phase control.

I. INTRODUCTION

Growing demand for high-power, high-efficiency, and high-density energy conversion in applications such as data center power delivery, grid-connected systems, and transportation electrification has driven interest in advanced converter topologies. Hybrid switched-capacitor (HSC) architectures have emerged as a compelling solution, offering high power density, high efficiency, and reduced device stress compared to many traditional power converters. These structures are often designed to distribute voltage stress across multiple switches, enabling the use of lower-voltage switching devices with improved figures of merit [1]. Maintaining this stress distribution requires flying capacitor voltages to remain near their nominal bias points. Problematically, many of these converter topologies are inherently non-deterministic under ideal conditions, and instead admit a continuum of steady-state solutions [2]. This unconstrained behavior increases susceptibility to disturbances and internal dynamics, which can cause significant deviations in flying capacitor voltages and potentially lead to device failure.

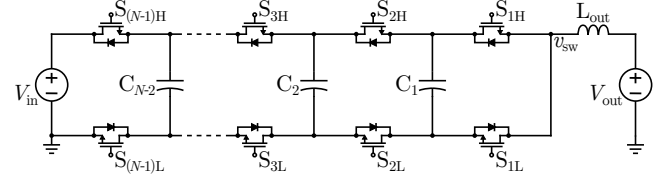


Fig. 1: N -level flying capacitor multilevel (FCML) converter schematic.

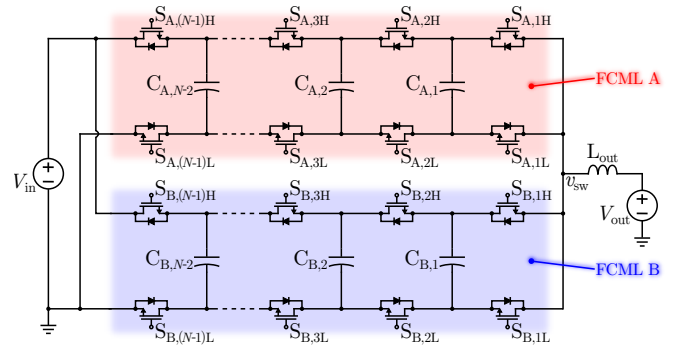


Fig. 2: Proposed N -level deterministic interleaved FCML (DI-FCML) converter schematic with its two constituent FCML capacitor networks highlighted.

Several approaches have been proposed to address these underlying dynamics and ensure proper capacitor balancing. Control-based approaches rely on modulation schemes or active voltage and/or current sensing with closed-loop control to regulate internal capacitor voltages in tandem with output regulation [3]–[7]. While effective in principle, these approaches often come at the expense of increased sensing and control complexity and may exhibit instability under light-load operation [3]. Alternatively, hardware-based approaches employ techniques such as balance boosters and coupled inductors to link converter stages and promote more favorable dynamics [8]. Work in [9] demonstrates that realistic loss mechanisms, such as switching losses, help drive the system towards a balanced state; however, this effect cannot be further leveraged in high-efficiency designs due to the associated increase in power dissipation.

In this work, we analyze the determinacy of the flying capacitor multilevel (FCML) converter (Fig. 1), given that this topology is well-known to have a strong sensitivity to line dis-

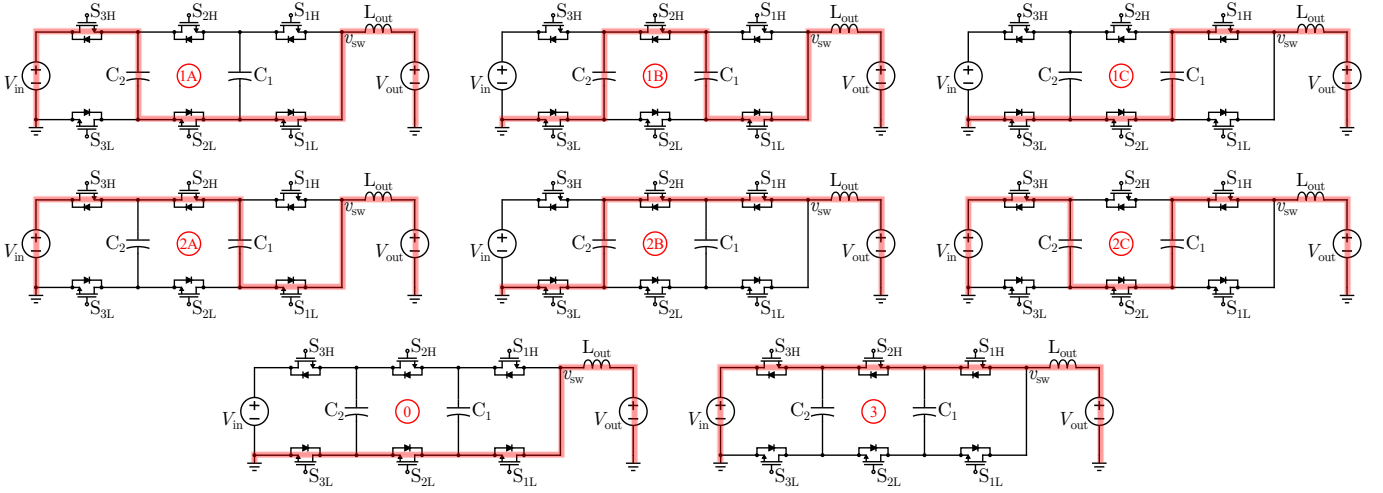


Fig. 3: All possible switch states of a conventional four-level FCML converter.

turbances. We then introduce a modified structure (Fig. 2) that is capable of maintaining full-rank determinacy of its flying capacitor voltages under both loaded and unloaded conditions, enabling automatic and rapid reconvergence following a transient event, while operating at a fixed-ratio output voltage. We further demonstrate that this modified structure—termed here as the *deterministic interleaved FCML* (DI-FCML)—can also preserve high-performance soft-charging operation [10] in steady-state without increasing switching activity.

II. THEORY

A. Indeterminacy of the FCML Converter

In a conventional FCML converter, every current path involving the flying capacitors also includes the output inductor—a deliberate feature that enables soft-charging operation. In other words, no switching state establishes a closed voltage loop among the flying capacitors that bypasses the output filter. This characteristic is observable in Fig. 3, which depicts all switching states of an example four-level FCML converter. This coupling causes the flying capacitor voltage dynamics to be fundamentally linked to the output-filter dynamics through the formation of switched LC networks with underdamped characteristics in high efficiency designs [2]. As a result of this direct coupling, following a line-voltage disturbance, the flying capacitor voltages cannot rebias through direct capacitor-to-capacitor interactions and must instead evolve through inductor-mediated current paths.

Table I presents an example 3:1 fixed-ratio switching sequence for a conventional four-level FCML converter along with the corresponding KVL equations. Notably, every KVL equation contains the time-varying output-inductor voltage, demonstrating that the capacitor-voltage dynamics cannot be decoupled from the output filter.

Since the output inductance is chosen suitably large so as to facilitate soft-charging operation, the resulting flying capacitor voltage response is inherently slow and underdamped. Subsequently, voltage imbalances may persist for many switching

TABLE I: Example 3:1 fixed-ratio switching sequence for the conventional FCML, and corresponding KVL equations.

Switching State	KVL Equation
(1A)	$V_{C2} + v_{L_{out}}(t) + V_{out} - V_{in} = 0$
(1B)	$-V_{C2} + V_{C1} + v_{L_{out}}(t) + V_{out} = 0$
(1C)	$-V_{C1} + v_{L_{out}}(t) + V_{out} = 0$

periods following a disturbance, leading to prolonged periods of uneven voltage stress across the converter switches.

Although realistic loss mechanisms and/or active balancing control can eventually drive the flying capacitor voltages toward their nominal operating points, the rate of convergence remains limited by the output-filter dynamics and competing control objectives. This motivates the development of converter structures capable of naturally self-establishing the desired flying capacitor voltage biases without relying on the output filter for charge redistribution.

B. Determinacy of the DI-FCML Converter

To address the issue of flying capacitor voltage balancing within the FCML converter, here we seek to structurally enforce state determinacy by introducing specific voltage loops without inductors into the converter's operating regime. Any voltage discontinuities within these imposed loops give rise to hard-charging inrush currents, which are leveraged to provide intrinsic feedback that rapidly drives the system toward a unique, deterministic steady-state operating point. Because these balancing interactions occur entirely within non-inductive voltage loops, the resulting flying capacitor voltage dynamics are dominated by the hard-charging interactions themselves and are effectively decoupled from the output-filter dynamics. As a result, following a line disturbance, the flying capacitors rapidly rebias to their nominal voltages. Importantly, this hard-charging loss mechanism is active only during transient rebiasing and is effectively absent in balanced steady-state, preserving the converter's overall efficiency. Moreover, because the balancing mechanism does

not rely on the output-filter current, its behavior is inherently independent of load, ensuring consistent operation from no-load to full-load conditions.

The conventional four-level FCML converter can be configured to operate in one of eight distinct switching states, illustrated in Fig. 3. Here, each of the two intermediate output voltage levels ($\frac{1}{3}V_{in}$ and $\frac{2}{3}V_{in}$) may be produced via three distinct switching states, (1A), (1B), (1C) and (2A), (2B), (2C). For a given conversion ratio, all three states must be used to maintain charge balance on the flying capacitors. In the proposed DI-FCML converter topology (Fig. 2) each of its two constituent FCML switched-capacitor networks—FCML A and FCML B—will progress through these switching states concurrently, but are never in the same state simultaneously (i.e., their phases are offset from one another). This interleaved and phase-shifted operation enables strategic interactions to occur among the flying capacitors, which are linked by a common switched-node, v_{sw} , effectively forming a series of capacitor voltage dividers that facilitate selective charge redistribution for automatic voltage balancing. This is the mechanism that will be leveraged to impose deterministic flying capacitor voltages.

To ensure determinacy, a switching sequence must be carefully selected such that, over one switching period, it generates N_C independent voltage equations that do not contain the output inductor, where N_C denotes the number of flying capacitors within the HSC network. Applying KVL around each capacitive loop formed throughout the switching period yields a linear system of equations whose unknowns are the capacitor voltages. A unique solution exists only if the resulting constraint matrix is full rank, requiring that the number of independent equations be equal to the number of unknowns.

For example, a four-level DI-FCML converter contains four flying capacitors and therefore requires four independent voltage constraints to uniquely determine its capacitor voltages. In the case of the DI-FCML converter, each switching state can impose only one constraining KVL equation, with the possibility that not all constraints are independent.

Fig. 4 illustrates one possible switching state of the four-level DI-FCML and highlights the corresponding non-inductive voltage loop. Because only a single such loop exists in this particular state, only one constraining KVL equation is obtained. Table II shows a viable 6-phase periodic switching sequence and its corresponding KVL equations for the proposed DI-FCML converter, operating with a 3 : 1 conversion ratio. (1) lists the same information in state-space format. The resulting system is full-rank (rank = 4), confirming deterministic flying capacitor voltages within the converter and automatic convergence to $V_{C_{A,2}} = V_{C_{B,2}} = \frac{2}{3}V_{in}$ and $V_{C_{A,1}} = V_{C_{B,1}} = \frac{1}{3}V_{in}$.

In addition to providing sufficient KVL constraints to ensure determinacy, the switching sequence must satisfy several other requirements. First, the two FCML networks must always be configured to present the same voltage at their shared switched

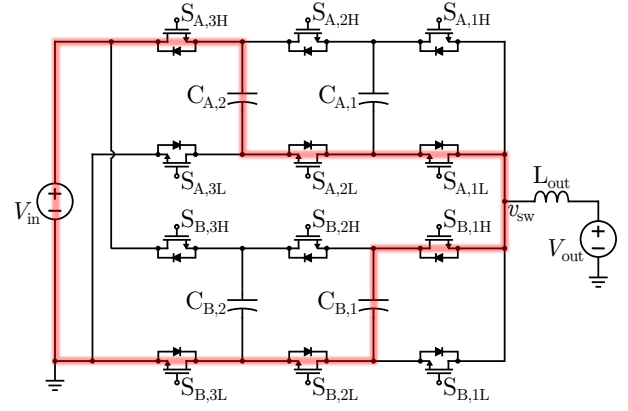


Fig. 4: (1A) : (1C) switching state for the four-level DI-FCML converter, with non-inductive voltage loop highlighted.

TABLE II: Example 3 : 1 fixed-ratio switching sequence for the DI-FCML (excluding split-phase states), and corresponding non-inductive voltage loop equations.

Phase	FCML A	FCML B	KVL Equation
ϕ_1	(1A)	(1C)	$V_{C_{A,2}} + V_{C_{B,1}} - V_{in} = 0$
ϕ_2	(1B)	(1A)	$-V_{C_{A,2}} + V_{C_{A,1}} - V_{C_{B,2}} + V_{in} = 0$
ϕ_3	(1C)	(1B)	$-V_{C_{A,1}} + V_{C_{B,2}} - V_{C_{B,1}} = 0$
ϕ_4	(1A)	(1B)	$V_{C_{A,2}} + V_{C_{B,2}} - V_{C_{B,1}} - V_{in} = 0$
ϕ_5	(1B)	(1C)	$-V_{C_{A,2}} + V_{C_{A,1}} + V_{C_{B,1}} = 0$
ϕ_6	(1C)	(1A)	$-V_{C_{A,1}} - V_{C_{B,2}} + V_{in} = 0$

$$\begin{bmatrix} 1 & 0 & 0 & 1 \\ -1 & 1 & -1 & 0 \\ 0 & -1 & 1 & -1 \\ 1 & 0 & 1 & -1 \\ -1 & 1 & 0 & 1 \\ 0 & -1 & -1 & 0 \end{bmatrix} \begin{bmatrix} V_{C_{A,2}} \\ V_{C_{A,1}} \\ V_{C_{B,2}} \\ V_{C_{B,1}} \end{bmatrix} + \begin{bmatrix} -1 \\ 1 \\ 0 \\ -1 \\ 0 \\ 1 \end{bmatrix} V_{in} = 0 \quad (1)$$

node when simultaneously active. Otherwise, contradictory switching states may create undesired hard-charging events and associated losses in steady-state operation. Second, all flying capacitors must satisfy charge balance over one switching period to ensure steady-state operation. Finally, switching activity should be minimized to reduce switching losses and implementation complexity.

C. DI-FCML Transient Response Analysis

Because the DI-FCML may rebias through imposed non-inductive voltage loops rather than solely through the output filter, the response of its flying capacitor voltages to a line-voltage disturbance is somewhat decoupled from load conditions. Considering only this intrinsic rebiasing mechanism, the rate at which the capacitor voltages converge to their new steady-state values is determined primarily by the switching frequency, where capacitor-to-capacitor interactions must be exercised. In practice, parasitic resistances introduce an additional dependence which limit the balancing currents exchanged between unbalanced capacitors, as per conventional *fast-switching-limit* behavior [11]. However, to provide analytical insight into the rebiasing process, these parasitic

effects are neglected in the following analysis—a reasonable assumption in high efficiency converter designs.

The following analysis focuses exclusively on the capacitor-voltage dynamics associated with the imposed non-inductive voltage loops. Specifically, the analysis considers the hard-charging interactions that occur between unbalanced flying capacitors during transient conditions. The effects associated with the output filter and load current are intentionally neglected, as they do not participate in the rapid charge-redistribution mechanism being investigated. Under these assumptions, the evolution of the flying capacitor voltages can be predicted analytically on a phase-by-phase basis, allowing the capacitor voltages at an arbitrary switching phase to be determined directly. The resulting model therefore characterizes the intrinsic rebiasing behavior of the DI-FCML.

Following an input-voltage disturbance, the flying capacitor voltages are no longer consistent with the KVL constraints imposed by the switching state. Consequently, at the beginning of an arbitrary phase, n , before any charge redistribution has occurred, the associated capacitor loop exhibits a KVL error. Let ϵ_n denote this error, defined as the amount by which the loop voltages fail to sum to zero. The KVL error for phase n can be computed using (2). In this expression, A and B are the state-space matrices, such as the ones defined in (1), and j denotes the row corresponding to phase n .

The KVL error associated with phase n is apportioned equally among the active flying capacitors, assuming identical capacitance values. Subsequently, each capacitor experiences an equal voltage adjustment—via hard-charging inrush currents—to resolve this KVL discontinuity. Let $N_{C,n}$ denote the number of flying capacitors participating in phase n . Under the mentioned assumptions, the flying capacitor voltages for phase n can be determined from those of the preceding phase, $n - 1$, using (3).

$$\epsilon_n = A_j \begin{bmatrix} v_{C_{A,N-2}} \\ v_{C_{B,N-2}} \\ \vdots \\ v_{C_{A,1}} \\ v_{C_{B,1}} \end{bmatrix}_{n-1} + B_j V_{in,n} \quad (2)$$

$$\begin{bmatrix} v_{C_{A,N-2}} \\ v_{C_{B,N-2}} \\ \vdots \\ v_{C_{A,1}} \\ v_{C_{B,1}} \end{bmatrix}_n = \begin{bmatrix} v_{C_{A,N-2}} \\ v_{C_{B,N-2}} \\ \vdots \\ v_{C_{A,1}} \\ v_{C_{B,1}} \end{bmatrix}_{n-1} - A_j^T \frac{\epsilon_n}{N_{C,n}} \quad (3)$$

Fig. 5 shows the analytically predicted evolution of the flying capacitor voltages in a four-level DI-FCML converter following an instantaneous 0V-to-30V input-voltage step, assuming the switching sequence defined in Table II. The disturbance introduces a mismatch between the capacitor voltages and the KVL constraints associated with each switching state, initiating a sequence of balancing events as the converter progresses through its switching cycle. With each switching phase, the corresponding KVL error is reduced through charge

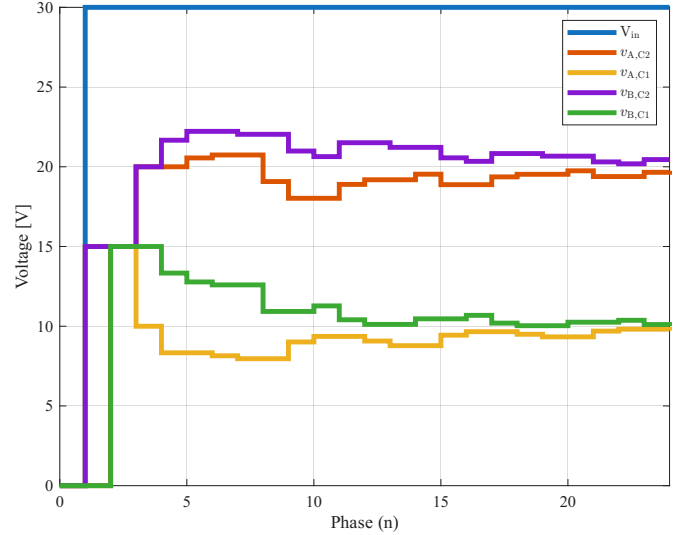


Fig. 5: Calculated flying capacitor voltage rebiasing trajectory in a four-level DI-FCML converter following an instantaneous 0V-to-30V input-voltage step, using the switching sequence of Table II.

redistribution among the flying capacitors, causing the voltage distribution to converge toward its new equilibrium. Notably, in this example, all flying capacitor voltages settle to within $\sim 2\%$ of their final values after 4 switching periods, demonstrating the rapid rebiasing capability of the proposed DI-FCML topology.

D. Split-Phase Switching in the DI-FCML

A consequence of the proposed control scheme is that when the DI-FCML is loaded, the flying capacitors within FCML A and FCML B may present different voltage ripple magnitudes to their common switched-node, violating KVL and resulting in unwanted hard-charging losses, even under steady-state conditions. To prevent this, we employ a modified clocking scheme, termed split-phase switching [12]–[14], to selectively introduce or remove specific capacitor branches within specific phase intervals, thereby avoiding voltage discontinuities and fully preserving soft-charging operation. We note that, in practice, split-phase timing must be adjusted as a function of load [15], due to the presence of non-zero inductor current ripple. Furthermore, [16] derives timing conditions that simultaneously account for both inductor current and flying capacitor voltage ripple, while [17] and [18] demonstrate approaches to closed-loop split-phase control.

III. EXPERIMENTAL RESULTS

To validate the theoretical framework developed in the previous section, a reconfigurable dual four-level FCML converter was designed and experimentally evaluated, as shown in Fig. 6. The hardware consists of two FCML switched-capacitor networks that share a common switched node and output filter, matching the circuit schematic of Fig. 2. By operating the two networks with identical switching sequences, the hardware functions as a conventional FCML converter with both capacitor networks operating completely in-phase. Alternatively,

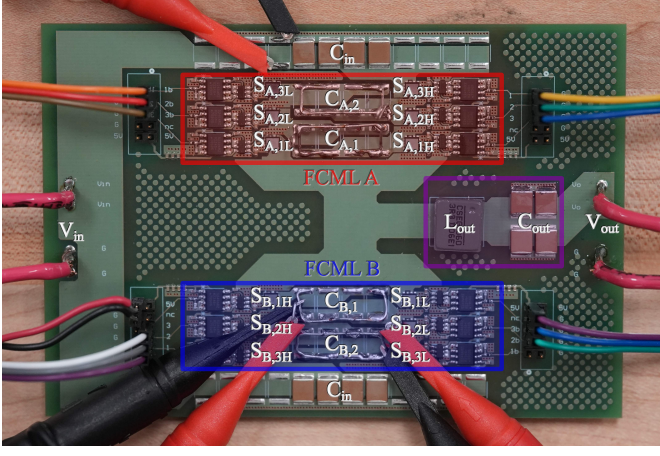


Fig. 6: Photograph of the reconfigurable FCML/DI-FCML converter hardware, with primary components labeled. Both FCML switched-capacitor networks A and B may be operated in phase to yield a single FCML converter through parallelization, or operated out of phase to yield *deterministic interleaved* operation.

TABLE III: Component details for hardware prototype.

Component	Details	Part Number
L_{out}	$3 \times 3.3 \mu\text{H}$	CSEG1060-3R3M
C_{in}	$8 \times 2.2 \mu\text{F X6S 2220}$	C5750X6S2W225K250KA
C_{out}	$4 \times 2.2 \mu\text{F X6S 2220}$	C5750X6S2W225K250KA
$C_{A,1-2}, C_{B,1-2}$	$8 \times 0.22 \mu\text{F C0G 1206}$	GRM31C5C1H224JE02L
$S_{A,1L-3L}, S_{A,1H-3H}$ $S_{B,1L-3L}, S_{B,1H-3H}$	$1.2 \text{ m}\Omega, 100 \text{ V}, 101 \text{ A}$	EPC2367
—	Gate Driver	LM5114BMF
—	Level Shifter	ADUM5240ARZ

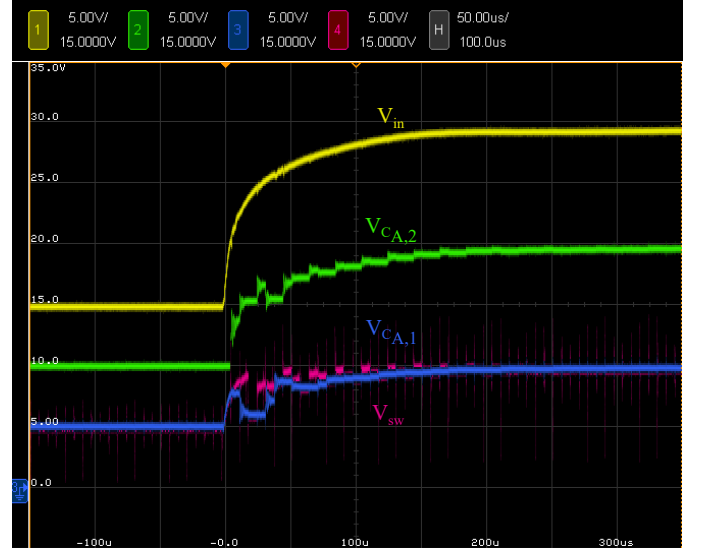
by operating the two networks with phase-shifted switching sequences, the hardware realizes the proposed deterministic interleaved FCML (DI-FCML) converter. This reconfigurable architecture enables direct experimental comparison between conventional FCML and DI-FCML operation using the same hardware platform with identical components. Table III lists the primary components used.

A. Rebalancing Comparison of the Switched-Capacitor Networks Only — Output Filter Disconnected

To validate the transient rebiasing analysis presented in Section II-C, a no-load input-voltage step test was conducted with the output filter intentionally disconnected. Under these conditions, the flying capacitor voltage dynamics are isolated from both load-current and output-filter effects, allowing the intrinsic rebiasing behavior of the switched-capacitor network to be observed directly. This operating condition closely matches the assumptions of the analytical model, which considers only the hard-charging interactions associated with the imposed non-inductive voltage loops. Furthermore, because conventional FCML converters rely on output-inductor-mediated dynamics to rebalance their flying capacitor voltages, removing the output filter provides a clear comparison of the fundamentally



(a)

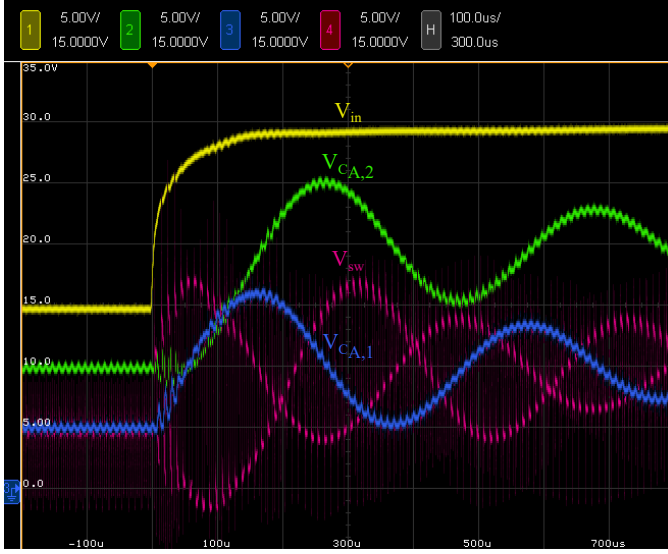


(b)

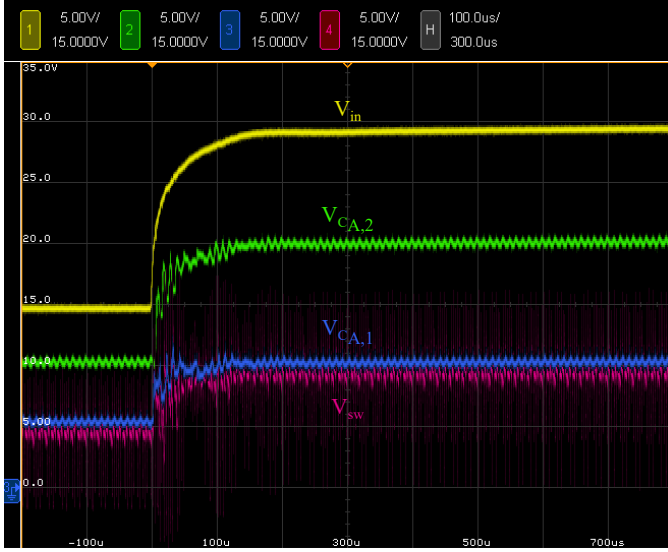
Fig. 7: (a) The conventional FCML converter failing to rebias and (b) the proposed DI-FCML converter rapidly and completely rebiasing in response to a 100% input voltage step, with no-load and output filter disconnected.

different rebiasing mechanisms present in the conventional FCML and proposed DI-FCML topologies.

For both the conventional FCML and DI-FCML converters, the input voltage was initially set to 15 V and both systems were allowed to reach steady-state, with the conventional FCML relying on parasitic losses to converge [9]. The input voltage was then stepped to 30 V, and the transient responses were recorded in Fig. 7. Over the same time interval, the flying capacitor voltages in the conventional FCML converter remain largely unchanged after the input voltage step, since it effectively has no means by which to rebias, absent an output inductor and associated return path. In contrast, by leveraging intrinsic hard-charging feedback, the DI-FCML converter's flying capacitors track changes in V_{in} and rapidly rebias to



(a)



(b)

Fig. 8: (a) The conventional FCML converter exhibiting slow and under-damped flying capacitor voltage rebiasing and (b) the proposed DI-FCML converter rapidly rebiasing in response to a 100% input-voltage step, under light-load operation with an output LC filter connected. $I_{Load} = 0.5$ A, $C_{fly} = 1.76$ μ F, and $L = 9.9$ μ H.

their new, correct steady-state voltages.

B. Rebalancing Comparison at Light-Load

Next, an LC filter was connected to the switch node of both the conventional FCML and DI-FCML converters, in addition to a 0.5 A load. Fig. 8 shows the resulting step response for both converters under the same input voltage disturbance conditions. The conventional FCML converter portrays the expected under-damped settling response [3], where the input voltage step induces oscillatory dynamics in the flying capacitor voltages, as charge piece-wise oscillates between them and the output LC filter. These oscillations are only weakly dampened by parasitic resistances in the circuit, resulting in significantly slower rebiasing compared to the DI-FCML case.

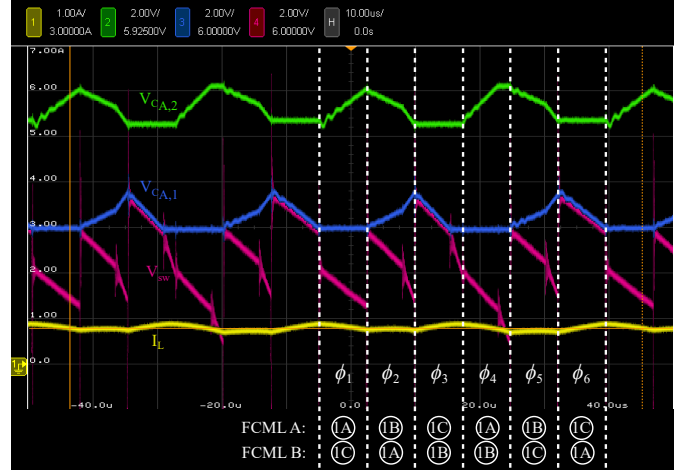


Fig. 9: DI-FCML waveforms displaying proper execution of split-phase switching in phases ϕ_2 , ϕ_3 , ϕ_4 , and ϕ_5 . The lack of abrupt changes in capacitor voltage verifies soft-charging operation.

In contrast, the DI-FCML converter again demonstrates rapid re-balancing of its flying capacitor voltages, with the system tracking changes in V_{in} and quickly converging to its new steady-state operating point.

Fig. 9 shows zoomed in waveforms of two flying capacitor voltages, the common switched-node voltage, v_{sw} , and output inductor current of the DI-FCML converter under split-phase operation at steady-state. The absence of any abrupt step-changes in the flying capacitor voltage waveforms demonstrates that the capacitors are being effectively soft-charged with split-phase control, even under loaded conditions.

IV. DISCUSSION

By leveraging deterministic balancing through strategic internal capacitor voltage loops, flying capacitors are able to rebias significantly faster than in conventional strategies, under both loaded and unloaded conditions. Rapid balancing reduces voltage stress on components, improving reliability and increasing immunity to transient input disturbances. Additionally, this approach eliminates the need for voltage or current sensing, simplifying implementation and reducing reliance on measurement and feedback circuitry. Importantly, requisite hard-charging is only present under transient events and is absent under steady-state operation, effectively preserving soft-charging operation for high conversion efficiency.

However, the DI-FCML converter topology requires twice the number of transistors and capacitors, although each process half the power as compared to the conventional FCML, allowing them to be half the size. As a result, the total volume of transistors and capacitors is expected to be comparable between the two topologies. That said, the DI-FCML requires twice the number of gate drivers and isolators, which may lead to reduced overall power density. Additionally, the DI-FCML converter's control scheme necessitates the use of split-phase switching, which is added complexity that the conventional FCML converter does not require.

Finally, while this work has focused only on fixed-ratio operation, the application of voltage regulation—including phase-shifted pulse-width modulation (PSPWM) schemes—to the DI-FCML converter is still currently under investigation.

V. CONCLUSION

This work presented a deterministic approach to capacitor voltage balancing within FCML converters through a proposed DI-FCML converter topology. A six-phase switching sequence for fixed-ratio conversion was introduced and its properties were analyzed. It was shown analytically that this switching sequence fully constrains the system, enforcing capacitor voltage determinacy within the converter.

To validate the proposed approach, a hardware prototype was designed and experimentally evaluated under different operating conditions. Experimental results demonstrate that the proposed topology rapidly rebalances flying capacitor voltage imbalances, while the conventional FCML converter struggled to achieve comparable rebalancing under the same conditions. Overall, the results indicated that the DI-FCML converter may provide a robust solution to the capacitor balancing problem for fixed-ratio conversion, enabling reliable operation independent of load conditions.

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